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IN THE CLAIMS

Please amend the claims as follows:

1. – 12. (Cancelled)

13. (Previously Presented) A computerized method of placing a plurality of components of an integrated circuit in a layout, the method comprising:

assigning each one of a plurality of components of an integrated circuit to one of a plurality of clusters;

generating a layout for each one of the plurality of clusters;

placing each one of the plurality of clusters in a layout for the integrated circuit wherein the placing is performed in a two-dimensional manner with a plurality of overlapping rows;

performing an analysis of the layout for the integrated circuit using a cost function having a reliability verification factor; and

automatically rearranging the layout for the integrated circuit by automatically rearranging the plurality of clusters; and

repeating the analyzing and the rearranging until the cost function is minimized.

14. (Original) The computerized method of claim 13, wherein the reliability verification factor represents the effects of electromigration and self heat.

15. (Original) The computerized method of claim 13, wherein a width of each one of the plurality of overlapping rows is a multiple of a smallest one of the plurality of clusters.

16. (Original) The computerized method of claim 14, wherein assigning each one of the components is performed based on a lumped gate ordering style.

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17. (Original) The computerized method of claim 14, wherein assigning each one of the components is performed based on a distributed gate ordering style.
18. (Original) The computerized method of claim 14, further comprising adjusting one or more of the plurality of components in one of the clusters to comply with a size constraint.
19. (Original) The computerized method of claim 18, wherein the adjusting is performed using device-based legging.
20. (Original) The computerized method of claim 18, wherein the adjusting is performed using stack-based legging.
21. (Original) The computerized method of claim 18, wherein the adjusting is performed using differential legging.
22. – 33. (Cancelled)
34. (Currently Amended) ~~The computerized method of claim 1, further comprising:~~ A computerized method of creating a layout for a circuit design performed by a computer aided design tool, the method comprising:
receiving a circuit design;
receiving at least one layout rule based on a reliability verification constraint;
assigning each transistor of the circuit design to a cluster, to produce multiple clusters;
generating a cluster layout for each cluster, to produce multiple cluster layouts wherein
generating the layout includes arranging the multiple ~~layout clusters~~ cluster layouts.; and
generating a circuit layout for the circuit design through computer automated operations;
performing an analysis of the circuit layout to determine whether the circuit layout
satisfies the at least one layout rule;

if the analysis indicates that the circuit layout does not satisfy a rule of the at least one layout rule, automatically rearranging portions of the circuit layout, to produce a revised circuit layout;

repeating the performing and automatically rearranging of the revised circuit layout until the revised circuit layout generated satisfies the at least one layout rule based on the reliability verification constraint received for the circuit design;

35. (Currently Amended) The computerized method of claim [[33]] 34, wherein automatically rearranging portions of the layout comprises:

automatically rearranging the multiple cluster layouts.

36. (Currently Amended) The computerized method of claim [[33]] 34, wherein assigning each transistor to a cluster comprises:

initially assigning each transistor to a preliminary cluster, resulting in multiple preliminary clusters;

merging the preliminary clusters to produce the multiple clusters; and

adjusting the multiple clusters.

37. (Currently Amended) The computerized method of claim [[33]] 34, wherein generating a cluster layout comprises:

building diffusion graphs for portions of the multiple clusters;

finding paths in the diffusion graphs; and

generating the multiple cluster layouts based on the paths.

38. – 39. (Cancelled)

40. (New) An article comprising:

a computer-readable medium including instructions that when executed cause a computer to:

assign each one of a plurality of components of an integrated circuit to one of a plurality of clusters;

generate a layout for each one of the plurality of clusters;

place each one of the plurality of clusters in a layout for the integrated circuit wherein the placing is performed in a two-dimensional manner with a plurality of overlapping rows;

perform an analysis of the layout for the integrated circuit using a cost function having a reliability verification factor; and

automatically rearrange the layout for the integrated circuit by automatically rearranging the plurality of clusters; and

repeat the analysis and the rearrange until the cost function is minimized.

41. (New) The article of claim 40, wherein the reliability verification factor represents the effects of electromigration and self heat.

42. (New) The article of claim 40, wherein a width of each one of the plurality of overlapping rows is a multiple of a smallest one of the plurality of clusters.

43. (New) The article of claim 40, wherein assigning each one of the components is performed based on a lumped gate ordering style.

44. (New) The article of claim 40, wherein assigning each one of the components is performed based on a distributed gate ordering style.

45. (New) The article of claim 40, further comprising adjusting one or more of the plurality of components in one of the clusters to comply with a size constraint.

46. (New) The article of claim 40, wherein the adjusting is performed using device-based legging.

47. (New) The article of claim 40, wherein the adjusting is performed using stack-based legging.

48. (New) The article of claim 40, wherein the adjusting is performed using differential legging.

49. (New) An article comprising:

a computer-readable medium including instructions that when executed cause a computer to:

receive a circuit design;

receive at least one layout rule based on a reliability verification constraint;

assign each transistor of the circuit design to a cluster, to produce multiple clusters;

generate a cluster layout for each cluster, to produce multiple cluster layouts wherein generating the layout includes arranging the multiple cluster layouts.; and

generate a circuit layout for the circuit design through computer automated operations;

perform an analysis of the circuit layout to determine whether the circuit layout satisfies the at least one layout rule;

if the analysis indicates that the circuit layout does not satisfy a rule of the at least one layout rule, automatically rearrange portions of the circuit layout, to produce a revised circuit layout;

repeating the performing and automatically rearranging of the revised circuit layout until the revised circuit layout generated satisfies the at least one layout rule based on the reliability verification constraint received for the circuit design;

50. (New) The article of claim 49, wherein automatically rearranging portions of the layout comprises:

automatically rearranging the multiple cluster layouts.

51. (New) The article of claim 49, wherein assigning each transistor to a cluster comprises:

initially assigning each transistor to a preliminary cluster, resulting in multiple preliminary clusters;

merging the preliminary clusters to produce the multiple clusters; and

adjusting the multiple clusters.

52. (New) The article of claim 49, wherein generating a cluster layout comprises:

building diffusion graphs for portions of the multiple clusters;

finding paths in the diffusion graphs; and

generating the multiple cluster layouts based on the paths.